CLAIMS

What is claimed is:

1. A method comprising:

(a) detecting whether a first clock signal is inadequate, wherein the first clock signal is generated by a first clock circuit;

(b) decoupling the first clock circuit from a system clock input lead of a processor;

(c) coupling a second clock circuit to the system clock input lead of the processor;

(d) enabling a third clock circuit;

(e) decoupling the second clock circuit from the system clock input lead of the processor; and

(f) coupling the third clock circuit to the system clock input lead of the processor.

2. The method of claim 1, wherein the first clock circuit is a high-speed, external crystal oscillator, wherein the second clock circuit is a low-speed, internal watchdog timer, and wherein the third clock circuit is a high-speed, internal oscillator.

3. The method of claim 1, wherein the detecting in (a) is performed by detecting no signal edges of the first clock signal during a time period over which a linear feedback shift register increments to a predetermined value.

4. The method of claim 1, wherein the decoupling the first clock circuit in (b) is not performed as a result of a signal from the processor.

5. The method of claim 1, wherein the coupling the second clock circuit in (c) is not performed as a result of a signal from the processor.

6. The method of claim 1, wherein the third clock circuit is enabled in (d) by powering up the third clock circuit.

7. The method of claim 1, further comprising, between step (a) and step (b):

(g) sending an interrupt signal to the processor indicating that the first clock circuit has failed.

8. The method of claim 1, further comprising, between step (a) and step (b):

(g) disabling a failure detection circuit that performed the detecting in (a).

9. The method of claim 1, further comprising, between step (d) and step (e):

(g) detecting whether a second clock signal is inadequate, wherein the second clock signal is generated by the third clock circuit.

10. The method of claim 1,

wherein the first clock circuit can be coupled to the system clock input lead by a multiplexer, the first clock circuit being coupled to a first data input lead of the multiplexer,

wherein the second clock circuit is coupled in (c) to the system clock input lead by the multiplexer, the second clock circuit being coupled to a second data input lead of the multiplexer,

wherein a third data input lead of the multiplexer is grounded, and

wherein between step (b) and step (c) the multiplexer couples the third data input lead of the multiplexer to the system clock input lead.

11. An integrated circuit, comprising:

(a) a processor with a system clock input lead;

(b) a terminal, the terminal coupled to a first clock circuit, the first clock circuit generating a first clock signal;

(c) a second clock circuit;

(d) a third clock circuit; and

(e) a clock controller coupled to the system clock input lead, wherein the clock controller is adapted to decouple the system clock input lead from the terminal and to couple the system clock input lead to the second clock circuit upon detecting that the first clock signal is inadequate, and wherein the clock controller is further adapted to turn on the third clock circuit upon detecting that the first clock signal is inadequate.

12. The integrated circuit of claim 11, wherein the first clock circuit is a high-speed external crystal oscillator.

13. The integrated circuit of claim 11, wherein the second clock circuit is a low-speed, internal watchdog timer oscillator.

14. The integrated circuit of claim 11, wherein the clock controller can decouple the system clock input lead from

the terminal when the processor is receiving an inadequate first clock signal.

15. The integrated circuit of claim 11, wherein the clock controller decouples the system clock input lead from the second clock circuit and couples the system clock input lead to the third clock circuit.

16. The integrated circuit of claim 11, wherein the clock controller comprises a primary clock source fail detect circuit, and wherein the primary clock source fail detect circuit detects whether the first clock signal is inadequate.

17. The integrated circuit of claim 16, wherein the clock controller further comprises a secondary clock source fail detect circuit, and wherein the secondary clock source fail detect circuit detects whether a second clock signal is inadequate, wherein the second clock signal is generated by the third clock circuit.

18. The integrated circuit of claim 16, wherein the clock controller comprises a plurality of substantially identical clock source fail detect circuits, and wherein each of the clock source fail detect circuits detects whether a different clock signal is inadequate.

19. A microcontroller integrated circuit operable with an external first clock circuit, the microcontroller integrated circuit comprising:

(a) a processor having a system clock input lead;

(b) a terminal for receiving a first clock signal generated by the external first clock circuit;

(c) a second clock circuit; and

(d) means for detecting whether the first clock signal is inadequate and, upon detecting that the first clock signal is inadequate, for decoupling the terminal from the system clock input lead and coupling the second clock circuit to the system clock input lead, wherein the means decouples the terminal from the system clock input lead and couples the second clock circuit to the system clock input lead without receiving any signal from the processor.

20. The microcontroller integrated circuit of claim 19, further comprising:

(e) a third clock circuit, wherein the means turns on the third clock circuit upon detecting that the first clock signal is inadequate.

21. The microcontroller integrated circuit of claim 20, wherein the means decouples the second clock circuit from the system clock input lead and couples the third clock circuit to the system clock input lead after the turning on of the third clock circuit.